# Speech Synthesizer — MEA8000

## DESCRIPTION

The MEA8000 is a 24-pin N MOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately in a Read-Only Memory. An efficient, easy-to-use speech editing and encoding system with EPROM programming capability, has been specially developed.

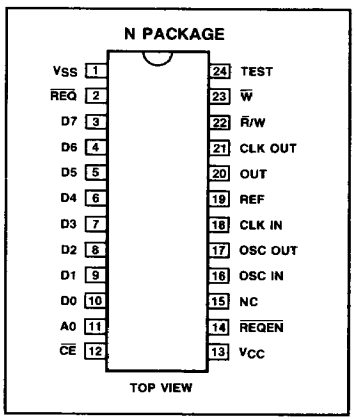
## APPLICATIONS

- Telephony
- Automotive
- Computer response/prompt.
- Video games.
- General industrial.

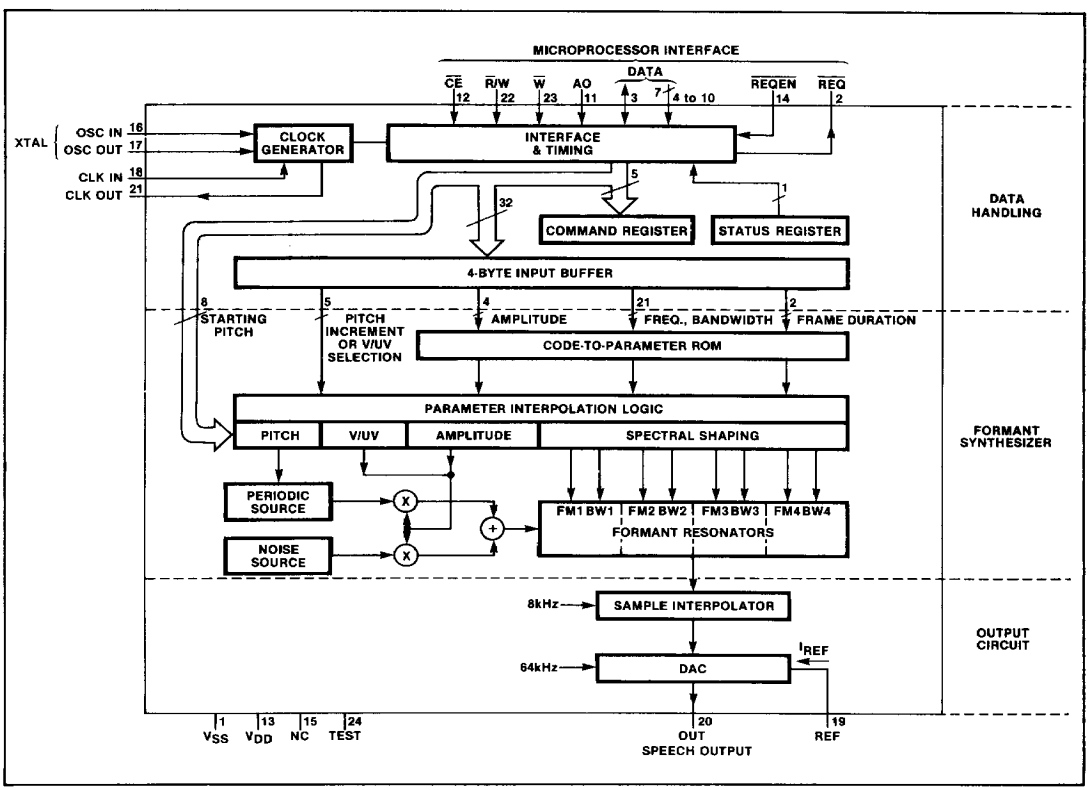
## FEATURES

- **Microprocessor interface cability including an 8-bit data bus, an enable and a read/write input control signals.**
- **32-bit data buffer holding speech frame codes.**
- **Digital filter of 8th order with 3 programmable formant frequencies, one fixed formant frequency, and 4 programmable formant bandwidths. 4 KH bandwidth.**
- **Programmable amplitudes.**
- **Programmable duration of each frame: 8, 16, 32, or 64 milliseconds.**
- **Low data rate: average 1000 bits/sec.**
- **Operates from standard EPROMs/ROMs.**
- **Minimal external audio filter requirement.**
- **Crystal controlled oscillator or external (TTL) clock.**
- **Single +5V power supply.**

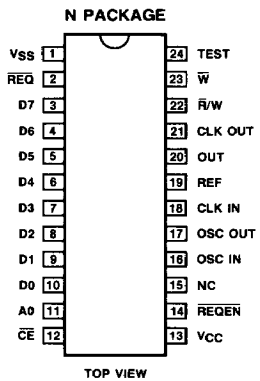
## PIN CONFIGURATION




## BLOCK DIAGRAM



## FUNCTIONAL PIN DESCRIPTION




| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| | | **CONTROL** |
| 2 | $\overline{REQ}$ | **DATA REQUEST** output signal (open drain) which follows the inverse of the status REQ bit, but only if enabled by either the ROE bit in the command register or the external $\overline{REQEN}$ input pin. |
| 3 to 10 | D7 to D0 | **Data bus** to which command or encoded speech parameters can be written. D7 is a bidirectional line through which the status bit can be read. |
| 11 | A0 | **Data/control** input. Discriminates between speech code input buffer (A0 = '0') and command register (A0 = '1') during a 'write' operation. |
| 12<br>22<br>23 | $\overline{CE}$<br>R/$\overline{W}$<br>$\overline{W}$ | **Chip enable, Read/Write, Write** These control signals provides an easy interface to most microprocessors or microcomputers (see timing diagrams). |
| 14 | $\overline{REQEN}$ | **Request enable** input. $\overline{REQEN}$ = '0' enables the status REQ bit to appear inverted on the $\overline{REQ}$ output, independent of the command register. |
| | | **TIMING** |
| 16<br>17 | OSC IN<br>OSC OUT | Connections for internal clock oscillator. Nominal crystal frequency is 3.84 MHz. OSC IN must be tied to ground if CLK IN is used. |
| 18<br>21 | CLK IN<br>CLK OUT | **Clock input** for external clock, TTL compatible, 3.84 MHz. Must be tied to ground when not used. A buffered output of the internal clock cycle (= CLK IN divided by 3). |
| | | **OUTPUT** |
| 19 | REF | **Reference Current** Input pin for biasing the audio output level. This reference current can be derived from a resistor to the positive supply. |
| 20 | OUT | **Speech output.** This output is a 64 kHz pulse, modulated in both width and amplitude. It is configured as a current sink with a saturating voltage of about 3V. |
| | | **SUPPLY** |
| 1 | $V_{SS}$ | **Ground.** |
| 13 | $V_{CC}$ | **Single supply voltage.** Nominally 5V, but battery operation is also possible. |
| 15 | NC | No connection. |
| 24 | TEST | Used for testing purposes. Changes other pin functions. Must be tied to ground for user operation. |

## ABSOLUTE MAXIMUM RATING

| SYMBOL AND PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | −0.5 to +7 | V |
| $V_I$ | Voltage on any pin with respect to $V_{SS}$ | −0.5 to +7 | V |
| $V_{\overline{REQ}}$, $V_{OUT}$ | Output voltage on pins 2 and 20 | 15 | V |
| $T_{STG}$ | Storage temperature range | −20 to +125 | °C |
| $T_A$ | Operating ambient temperature range | 0 to +70 | °C |

## DC ELECTRICAL CHARACTERISTICS $T_A$ = 25°C: $V_{CC}$ = 5V, unless otherwise stated. All voltages referenced to $V_{SS}$

| SYMBOL AND PARAMETER | | TEST CONDITION | MEA8000 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage (note 1) | | 4.5 | 5.0 | 5.5 | V |
| $I_{CC}$ | Supply current | (No audio load) | | 30 | 50 | mA |
| | D0 to D7, A0, $\overline{CE}$, $\overline{W}$, $\overline{R}$/W, $\overline{REQEN}$, CLK IN: | | | | | |
| $V_{IH}$ | Input HIGH voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW voltage | | −0.5 | | 0.8 | V |
| $I_{IR}$ | Input Leakage current (note 2) | | | | 10 | μA |
| $C_I$ | Input Capacitance | | | | 7 | pF |
| | D7 (I/O) , CLK OUT: | | | | | |
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = −100 μA | 2.4 | | | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $C_L$ | Output Load capacitance | | | | 50 | pF |
| | $\overline{REQ}$: | | | | | |
| $V_{OH}$ | Output HIGH voltage | Open drain | | | 13.2 | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $C_L$ | Output Load capacitance | | | | 50 | pF |
| | Audio output | | | | | |
| $I_{REF}$ | Reference current (note 8) - Pin 19 | | | | 0.3 | mA |
| $I_{OUT}$ | Output current (peak) - Pin 20 | | | | | |
| | | $I_{REF}$ = 0 mA | | 100 | | μA |
| | | $I_{REF}$ = 0.1 mA | | 1.7 | | mA |
| | | $I_{REF}$ = 0.3 mA | | 5 | | mA |
| $V_{OUT}$ | $V_{OUT}$ (pin 20) for linear operation (note 3) | $I_{REF}$ = 0.1 mA | 2.5 | | 13.2 | V |
| | Oscillator | | | | | |
| $f_{XTAL}$ | Crystal frequency | Internal | | 3.84 | 4.00 | MHz |
| $f_{CLK}$ | Clock frequency | External | | 3.84 | 4.00 | MHz |

NOTES
1. The circuit will continue to operate from a supply of up to 6.5V, but without necessarily meeting the specification.
2. This is also valid for $V_{CC}$ = 0V.
3. This permits connection of the output load to a supply higher than that supplying the synthesizer.

## AC ELECTRICAL CHARACTERISTICS (note 4) (Figure 4 and 5)

| SYMBOL AND PARAMETER | TEST CONDITION | MEA8000 | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $t_{WR}$ Write enable pulse width. | Clock frequency = 3.84 MHz | 200 | | | ns |
| $t_{AS}$ Address set-up time. | | 30 | | | ns |
| $t_{AH}$ Address hold time. | | 30 | | | ns |
| $t_{DS}$ Data set-up time for write operation. | | 150 | | | ns |
| $t_{DH}$ Data hold time for write operation. | | 30 | | | ns |
| $t_{RH}$ Request hold time (note 5) | | | | 350 | ns |
| $t_{RN}$ Request next (note 6) | | | | 3 | µs |
| $t_{RD}$ Read enable time. | | 200 | | | ns |
| $t_{DD}$ Data delay for read operation (note 7) | | | | 150 | ns |
| $t_{DF}$ Data floating for read operation (note 7) | | | | 150 | ns |
| $t_{RV}$ Request valid before a write operation. | | 0 | | | ns |
| $t_{ROE}$ Request output enable response. | | | | 750 | ns |
| $t_{CS}$ Control set-up time. | | | | 20 | ns |
| $t_{CH}$ Control hold time. | | | | 20 | ns |

NOTES

4. Timing reference level is 1.5V.
5. An external pull up resistor is required, as this is an open drain output. The time ($t_{RH}$) to reach 2.0V is specified at a load to 5V of 3.3 kΩ and 50 pF.
6. Between two data write operations of one speech frame.
7. Levels greater than 2.0V for a '1' or less than 0.8V for a '0' are reached with a load of one TTL input and 50 pF.
8. Typical voltage level at the REF pin is 2.5V.

5

# Speech Synthesizer | MEA8000

## PRINCIPLE OF OPERATION

The MEA8000 voice synthesizer implements the vocal tract modeling technique of voice synthesis (also known as formant synthesis). This technique results in producing good quality speech with the lowest possible bit rates; this will in turn mean small memory size requirements.

Figure 1 shows an electronic model of the human vocal tract. A mixture of a periodic signal, representing the pitch of the original speech, and an aperiodic signal, representing the unvoiced sound in the speech, is fed via an amplifier stage to a variable filter comprising of four resonators. The amplifier controls the amplitude of the synthesized sound while the resonators model the sound in accordance with the formants in the original speech. Each resonator is controlled by two parameters, one for the resonant frequency and one for the bandwidth. The information required to control such a synthesizer system is defined by the pitch frequency, the amplitude values, the voiced/unvoiced source selection and the resonator settings. By periodic updating of this control information one can obtain a good replica of the original speech.

### Operation

The MEA8000 generates speech output by suitable filtering of a relatively low frequency sawtooth waveform for voiced sounds or for random noise for unvoiced sounds.

Speech encoded parameters, controlling the on-chip periodic source and digital filter, are transmitted on the 8-bit data bus from external memory to the MEA8000 under the control of an external microprocessor or microcomputer.

At first, a byte containing the starting pitch code must be transmitted to the MEA8000. This byte goes directly to the pitch generating circuitry via the input interface logic. Subsequent pitch frequencies are then specified using the pitch increment parameter; this method of encoding pitch contributes to the low bit rate requirements.

After receiving the starting pitch code, the codes of each speech frame (32 bits), when received, are shifted into a four-byte input buffer before being translated into control parameters by the code-to-parameter ROM (See Block Diagram). The parameter interpolation logic calculates the difference, and interpolates linearly between consecutive parameters to smooth the parameter transients. The interpolation interval is decoded using the two Frame Duration (FD) bits in each speech frame. Because the FD bits specify a frame duration of 8, 16, 32 or 64ms, the resulting average bit rate is about 1000 bits/sec.

Since the on-chip output sampling rate is 64KHz, the need for an external analog output filter is greatly reduced.

**Modes of Operation**

1. STOP mode: characterized by a silent output and the status REQ bit set to '1'. This mode is entered from power up or by STOP command. The mode is entered automatically if at the end of an active speech frame the next four parameter bytes are not yet received while the CONT bit in the command register is a '0'. In the latter case the final speech frame will be repeated once but with a decaying amplitude and the same pitch.

2. ACTIVE mode: a speech sample is being produced.

3. CONTINUOUS mode: entered if an active speech frame is finished and new data is not supplied in time while the CONT bit in the command register is a '1'. The synthesizer will repeat the last speech frame indefinitely until all four new data bytes are received, a STOP command has been issued or the CONT command bit has been reset.

### Control Signals

With the three control signals $\overline{CE}$, $\overline{W}$ and $\overline{R}/W$, provided on 3 external pins, the MEA8000 voice synthesizer chip is made compatible with most popular microprocessors and microcomputers. Please refer to the timing diagrams for timing requirements.

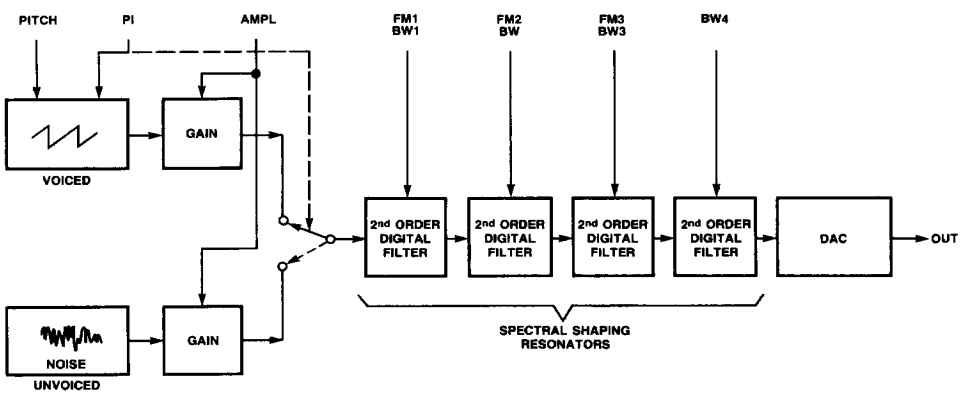



**Figure 1. Electronic Model of Human Vocal Tract.**

## Addressing the MEA8000

The MEA8000 voice synthesizer chip is addressed as a peripheral device to the host microprocessor or microcomputer. The three control signals, $\overline{CE}$, $\overline{W}$, and $\overline{R/W}$ along with the A0 address input, allow the MEA8000 to be addressed as an I/O device or as a memory device in a memory-mapped I/O system.

The input buffer and the command register are write-only while the status register is a read-only, as depicted in the following table:

| $\overline{CE}$ | $\overline{W}$ | $\overline{R/W}$ | A0 | OPERATION |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | Write Data |
| 0 | 0 | 1 | 1 | Write Command Register |
| 0 | X | 0 | X | Read Status Register |
| 0 | 1 | 1 | X | Three-State Data Bus |
| 1 | X | X | X | Three-State Data Bus |

## Status Register

The MEA8000 status register consists of a single bit: REQ. The status REQ bit appears on bit 7 of the data bus, D7, when reading the status register. The $\overline{REQ}$ output carries the inverse polarity of the status REQ bit. When the status REQ bit is a "0", the MEA8000 is busy and cannot accept any write data. The MEA8000 requests more data by setting its status REQ bit to a "1"; in this case the $\overline{REQ}$ output pin is active "0" only if this output is enabled. The $\overline{REQ}$ output is enabled either by hardware by connecting $\overline{REQEN}$ pin to ground, or by software by setting the ROE bit in the command register to a "1" while holding $\overline{REQEN}$ pin high. The MEA8000 voice synthesizer chip can then be used in an interrupt driven environment or in a polled type structure.

## Speech Code Input Buffer

The MEA8000 has a 32-bit (4-byte) input buffer. This buffer holds the speech encoded parameters for one speech frame.

Starting from the STOP mode — see Modes of Operation — the first data byte received by the MEA8000 will be interpreted as a starting value for the pitch. Every four successive data bytes received thereafter are treated as a group of speech code. The coded speech frame format is shown in Figure 2.

Writing a data byte into the MEA8000 will, automatically, clear the status REQ bit to "0". Within a group of 4 bytes (i.e. one speech frame), the $\overline{REQ}$ output (if enabled) will be activated within 3µs, measured from the trailing edge of $\overline{CE}$ or $\overline{W}$ (depending on which is used as the write strobe — see Timing), indicating a request for the next byte within the same group. Note that this time is extended to a multiple of 8ms (8, 16, 32 or 64) after writing the fourth, or last, byte of a group. This allows the host microprocessor enough time to use polling, instead of interrupts, since the minimium time of a speech frame is 8ms.

When in the STOP mode, the MEA8000 voice synthesizer will commence producing sound after receipt of 5 bytes (Figure 2).

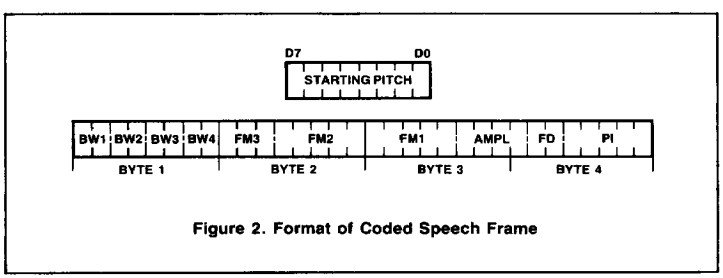



**Figure 2. Format of Coded Speech Frame**

| SYMBOL AND PARAMETER | | BITS |
|---|---|---|
| Starting Pitch | Initial value for pitch | 8 |
| FD | Speech frame duration | 2 |
| PI | Pitch increment (rate of pitch change) or noise selection | 5 |
| AMPL | Amplitude | 4 |
| FM1 | Frequency of 1st formant | 5 |
| FM2 | Frequency of 2nd formant | 5 |
| FM3 | Frequency of 3rd formant | 3 |
| FM4 | Frequency of 4th formant (fixed at 3500 Hz) | 0 |
| BW1 | Bandwidth is 1st formant | 2 |
| BW2 | Bandwidth of 2nd formant | 2 |
| BW3 | Bandwidth of 3rd formant | 2 |
| BW4 | Bandwidth of 4th formant | 2 |

## Command Register

The MEA8000 has a 5-bit command register. A command word is written into the command register by performaing a write operation with A0 input being set to "1".

The following explains the various command bits in the command register:

STOP results in an immediate reset of the synthesizer to the STOP mode. The ROE and CONT are not affected by this command.

CONT Continuous mode. This bit can be set or cleared only if the corresponding CONT enable bit is programmed as a '1'. In the continuous mode the synthesizer will not revert to the STOP mode if all four parameters are not received before the end of the current speech frame, but will repeat it indefinitely.

If CONT = '0', the last frame will be repeated once with decaying amplitude and the same pitch before the stop mode is entered.

ROE Request Output Enable. This bit can be set or cleared only if the corresponding ROE enable bit is a '1'. ROE determines whether the request in the status bit appears on the REQ pin. Note: the same can be achieved by connecting the REQEN pin (request enable) to a '0'.

After power on, the command register bits CONT and ROE will both be zero. Thus power on equals the command 00011010 = 1 A (hexadecimal).

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| | | | STOP | CONT enable | CONT | ROE enable | ROE |
| Not used | | | '0' = No action<br>'1' = Stop | 00 = No action<br>01 = No action<br>10 = Slow stop<br>11 = Continue | | 00 = No action<br>01 = No action<br>10 = Disable $\overline{REQ}$ output<br>11 = Enable $\overline{REQ}$ output | |

## ROM Mapping

The external ROM that stores the speech codes of an utterance or a word (called a speech file) also stores the starting pitch byte and the file header. The header comprises three bytes, two that indicate the number of bytes in the file and one that allows additional data to be encoded for each file.

Usually, more than one speech file will be stored in a ROM. An index is made by listing the 2-byte starting addresses of each file at the beginning of the ROM. The end of the index is indicated by the bytes FF FF. Figure 3 shows examples of ROM mapping.

## Power Supply

During (slow) power-up or power-down, the MEA8000 voice synthesizer will not produce any spurious sound. When powering-up the device, the MEA8000 will be in the STOP mode with command bits ROE and CONT being set to "0".

## Speech Editing and Encoding System

A specially designed speech editing and encoding system, targeted for use with the MEA80000, has been developed. The system consists of a Speech Adapter Box (SAB), a customized software package, and a general purpose personal computer.

The system is capable of programming the PROM's with the most efficient speech parameters. These parameters, when read by the MEA8000 voice synthesizer chip, will produce the best quality speech possible that this chip is capable of delivering.

## Timing Diagrams

Read and write timing diagrams are depicted in Figures 4, 5, and 6. Note that for a read operation, either $\overline{CE}$ or R/$\overline{W}$ can be used as the read strobe whereas for a write operation, either $\overline{CE}$ or $\overline{W}$ can be used as the write strobe. This allows great flexibility in system design.

Figure 7 shows the timing sequence encountered when writing speech code data into the MEA8000. In the figure, data is written on the rising edge of $\overline{CE}$. Starting in the STOP mode, the first byte to be written is the starting pitch. This is followed by 4 consecutive bytes, representing the first speech frame to be written into the MEA8000. Note that within the same frame, $\overline{REQ}$ output pin (if enabled) is activated within 3µs indicating, to the host microprocessor, its readiness to accept the next byte. After receiving the fourth byte of a speech frame, the $\overline{REQ}$ output pin will not be activated until the frame duration period (specified by the two FD bits) has elapsed. This time is equivalent to 8, 16, 32 or 64ms.

## System Configurations

Figure 8 shows a minimal system configuration for a voice application system using a general purpose microprocessor or a single chip microcomputer. In the latter case, speech code parameters are stored in the on-chip microcomputer ROM.

Figure 9 depicts a speech synthesis system using the SCN8051, 8-bit single chip microcomputer. Separate external program memory and speech parameters memory is shown, using 64K ROM chips. Note that external buffers might be needed on P0 (0-7) depending on loading conditions.

Figure 10 shows a typical audio output stage configuration using the TDA1011 audio power amplifier chip while Figure 11 depicts an audio output stage for 8 ohm speaker using discrete components.

The oscillator/clock configurations are depicted in Figure 12.

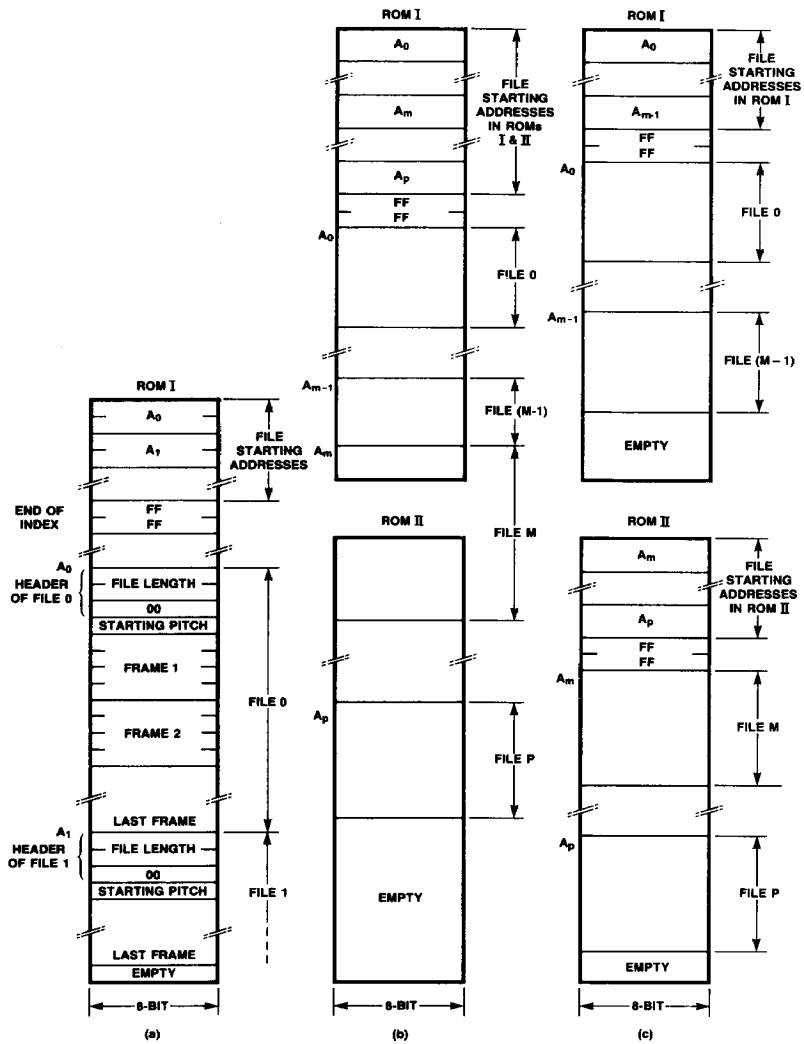



**Figure 3. Examples of ROM Memory Mapping; (a) Vocabulary in One ROM, (b) and (c) Vocabulary in Two ROMs.**

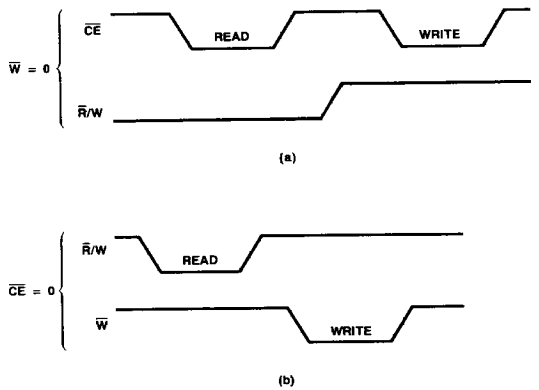



**Figure 4. (a) Chip Enable (CE) Used as a Read or Write Strobe; (b) Separate Read and Write Strobes.**

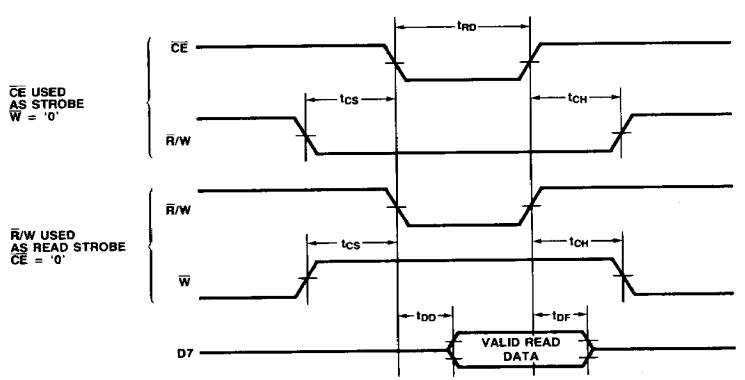



**Figure 5. Read Timing**

NOTES
Address input A0 is a don't care. Data bits D0 to D6 remain floating.

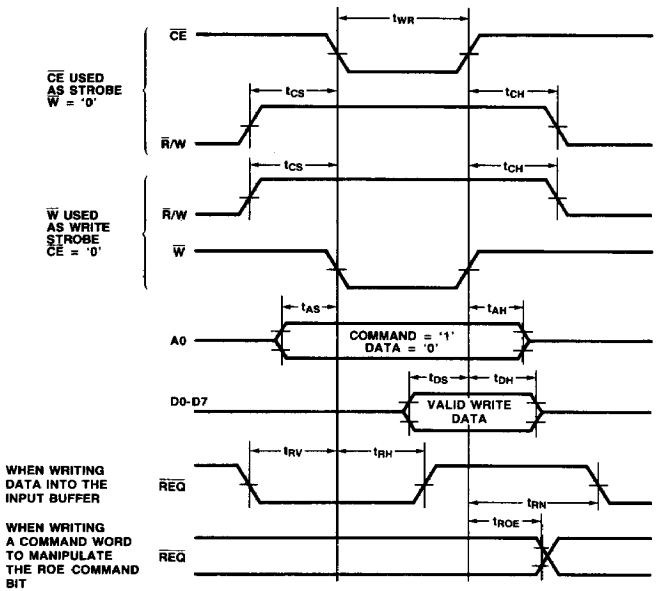



**Figure 6. Write Timing**

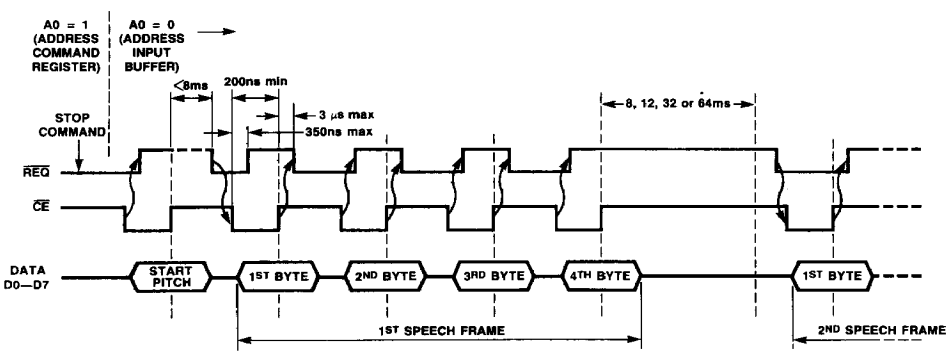
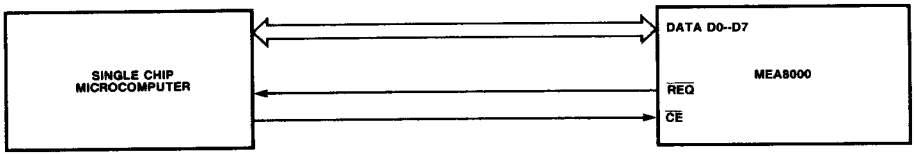
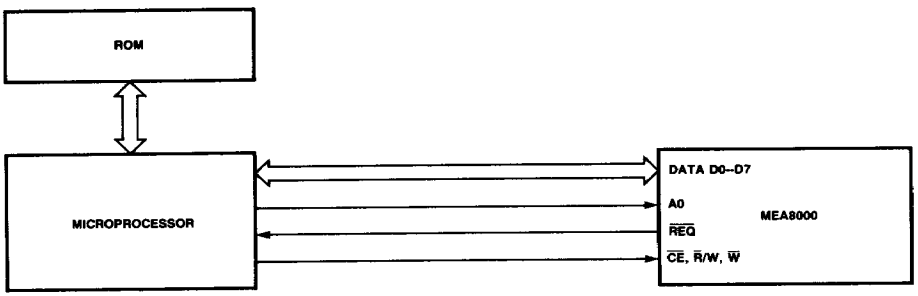


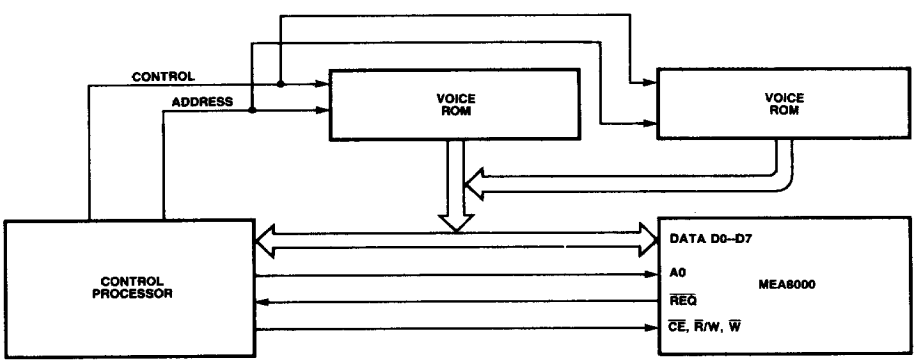

**Figure 7. Speech Code Data Write Timing Sequence**




a. Minimal System: Single Chip Microcomputer With On-chip Voice ROM.




b. MEA8000 as a Microprocessor Peripheral




c. Applications Using Separate Voice ROMs.

Figure 8. Typical Application Configurations.

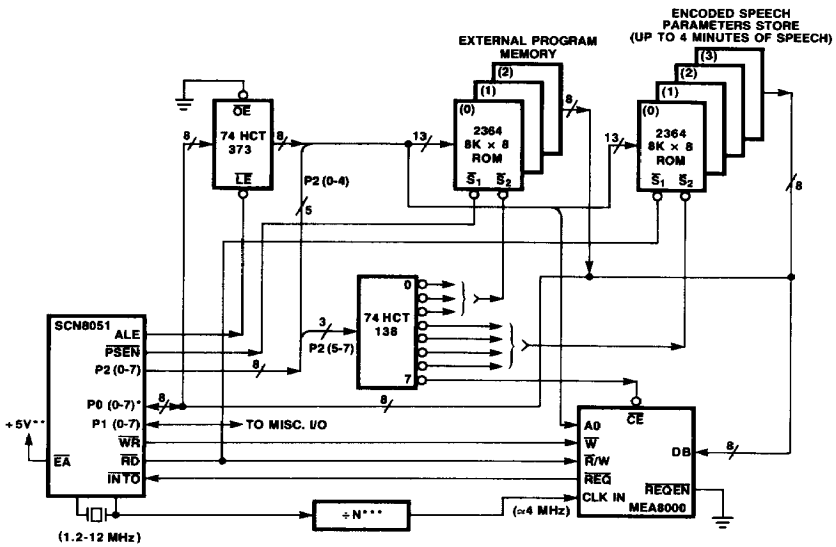



**Figure 9. Speech Synthesis System Using the 8051 8-Bit Microcomputer**

*External buffers might be needed.

**Connect EA to ground for the ROM less version (SCN 8031).

*** ÷N is a single F/F when XTAL frequency is around 8 MHz

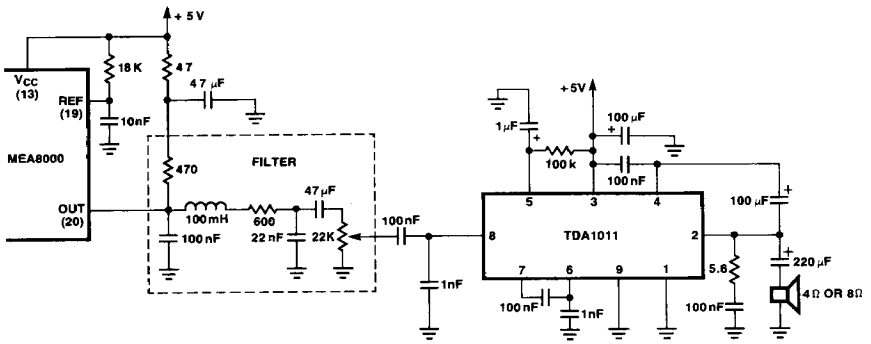



Figure 10. Audio Output Stage—Typical Configuration

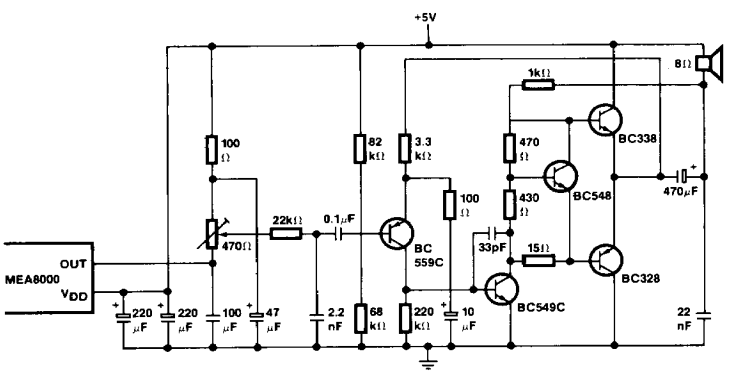



Figure 11. Audio Output Stage Using Discrete Components (8Ω Speaker)

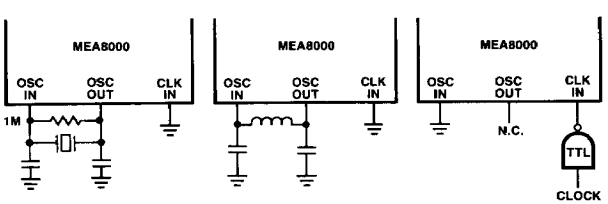



Figure 12. Oscillator/Clock Configurations